AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (previously presented): An image processing system provided with a field programmable gate array which is capable of altering an internal logic description, said description prescribing operation during an operating state, wherein an image processing method of said image processing system comprises:

executing digital image processing of an interval of active pixel in the condition that a first internal logic description is written in said field programmable gate array;

executing digital control processing in the condition that said first internal logic description of said field programmable gate array is rewritten to a second internal logic description in an interval of non-active pixel with the exception of said interval of active pixel; and

executing digital image processing again in the condition that said second internal description is rewritten to said first internal logic description;

wherein all operations necessary to perform said digital image processing and said digital control processing are performed in said field programmable gate array.

2. (original) An image processing system as claimed in claim 1, wherein there is provided an image pick-up element, and said image processing system executes color signal processing of picked-up image by said image pick-up element during said interval of active pixel, while during said interval of non-active pixel, said image processing system executes said digital control processing in relation to said color signal processing.

3. (original) An image processing system as claimed in claim 1, wherein said interval of non-active pixel is a vertical blanking interval.

4. (original) An image processing system as claimed in claim 1, wherein said interval of non-active pixel is a horizontal blanking interval.

5. (original) An image processing system as claimed in claim 1, wherein said image processing system executes image compression processing in said interval of active pixel, and said image processing system executes digital control processing in relation to said image compression processing in said interval of non-active pixel.

6. (original) An image processing system as claimed in claim 1, wherein said digital control processing is code quantity control processing.

7. (original) An image processing system as claimed in claim 2, wherein said interval of non-active pixel is a interval of optical black pixel of said image pick-up element.

8. (original) An image processing system as claimed in claim 2, wherein said digital control processing is an automatic white balance control processing.

9. (original) An image processing system as claimed in claim 2, wherein said digital control processing is an auto-focus control processing.

10. (original) An image processing system as claimed in claim 2, wherein said digital control processing is an automatic lightness control processing.

11. (previously presented): An image processing method for altering an internal logic description prescribing operation during an operating state comprising:

executing digital image processing of an interval of active pixel in the condition that a first internal logic description is written in a field programmable gate array;

executing digital control processing in the condition that said first internal logic description of said field programmable gate array is rewritten to a second internal logic description in an interval of non-active pixel with the exception of said interval of active pixel; and

executing digital image processing again in the condition that said second internal description is rewritten to said first internal logic description;

wherein all operations necessary to perform said digital image processing and said digital control processing are performed in said field programmable gate array.

12. (previously presented) An image processing method as claimed in claim 11, further comprising:

executing color signal processing of an image picked up by an image pick-up element during said interval of active pixel; and

executing said digital control processing in relation to said color signal processing during said interval of non-active pixel.

13. (previously presented) An image processing method as claimed in claim 11, wherein said interval of non-active pixel is a vertical blanking interval.

14. (previously presented) An image processing method as claimed in claim 11, wherein said interval of non-active pixel is a horizontal blanking interval.

15. (previously presented) An image processing method as claimed in claim 11, further comprising:

executing image compression processing in said interval of active pixel; and

executing digital control processing in relation to said image compression processing in said interval of non-active pixel.

16. (previously presented) An image processing method as claimed in claim 11, wherein said digital control processing is code quantity control processing.

17. (previously presented) An image processing method as claimed in claim 12, wherein said interval of non-active pixel is an interval of optical black pixel of said image pick-up element.

18. (previously presented) An image processing method as claimed in claim 12, wherein said digital control processing is an automatic white balance control processing.

19. (previously presented) An image processing method as claimed in claim 12, wherein said digital control processing is an auto-focus control processing.

20. (previously presented) An image processing method as claimed in claim 12, wherein said digital control processing is an automatic lightness control processing.

21. (new): An image processing system provided with a field programmable gate array which is capable of altering an internal logic description, said description prescribing operation during an operating state, wherein an image processing method of said image processing system comprises:

executing digital image processing of an interval of active pixel in the condition that a first internal logic description is written in said field programmable gate array;

executing digital control pre-processing or post-processing relating to said image processing in the condition that said first internal logic description of said field programmable

gate array is rewritten to a second internal logic description in an interval of non-active pixel with the exception of said interval of active pixel; and

executing digital image processing again in the condition that said second internal description is rewritten to said first internal logic description.

22. (new): An image processing system as claimed in claim 21, wherein said digital image processing and said digital control pre-processing or post-processing occur in one frame.